

Introduction

The following document details the timing system within NetPod 4000 used to maintain synchronisation of the analogue data acquisition operations and also a summary of the Sigma Delta converters used to read the analogue input signals for on the analogue input modules. The aim of the document is really only a simple introduction on the operations of Sigma Delta ADC.

Summary

The Sigma delta converter considerably over samples the input signal at a rate much greater than specified by Nyquist theory to recover the input signal characteristics. Any out of bound interference is prevented from aliasing back into the area of interest by the on board digital anti-alias and data decimation filter.

A precision reference oscillator is used to pass timing signals to all of the Sigma Delta converters simultaneously therefore guaranteeing that the input channels acquire data at exactly the same instant in time. The analogue inputs are absolutely synchronised within the instrument.

Only very simple RC filters are utilised on the inputs to the ADC to prevent out of band signals from contaminating the results.

Analogue Input Modules

In order to explain how the NetPod 4000 makes synchronised data acquisition operations a schematic of a standard analogue input module. Each analogue input contains essentially the same components namely, a Sigma Delta ADC, precision reference voltage and an opto-isolator.

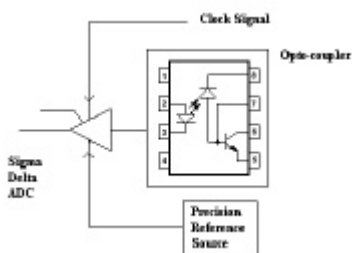


Figure 1 Schematic Of Individual Analogue Input

Not included in this technical note are details on how Keynes Controls adjusts the input impedance of the analogue modules using input amplifiers that vary on the different analogue interfaces.

The precision reference source is used to calibrate the Sigma Delta ADC.

The Opto-isolator provides the input protection to the analogue interface and enables high common mode inputs to be handled safely by the instrument.

The timing signal is used to synchronise the ADC.

Instrument ADC Timing

Figure 2 shows a basic schematic for the full system timing used within the NetPod 4000. A precision crystal oscillator on the DSP card is used to pass timing signals to all of the input modules simultaneously.

The timing signal is at a frequency of 10 MHz and is directly connected to the Sigma Delta ADC.

The Sigma Delta converter uses the the clock signal to synchronise its internal operations.

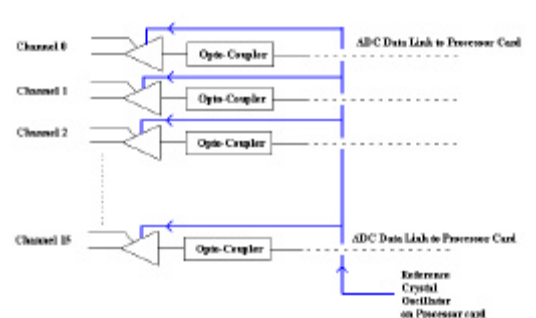


Figure 2 System Timing Diagram

Sigma Delta Data Acquisition

All Sigma Delta converters utilise very similar systems configuration as shown in Figure 3. Essentially the programmable gain amplifier and the sample of ADC sample rate are mathematically related such that the higher the gain of the amplifier, the lower the sample rate of the ADC that is allowed.

Figure 3 shows the basic schematic layout of the Sigma Delta Converter. The programmable gain amplifier is used to alter the input amplitude in order to achieve the best measurement. The high speed ADC makes measurements of the input signal at rate that is highly over sampled than that required by Nyquist theory to recover the input signal characteristics, for example, to make a measurement of 1 Hz the ADC will be taking approximately 15,000 readings.

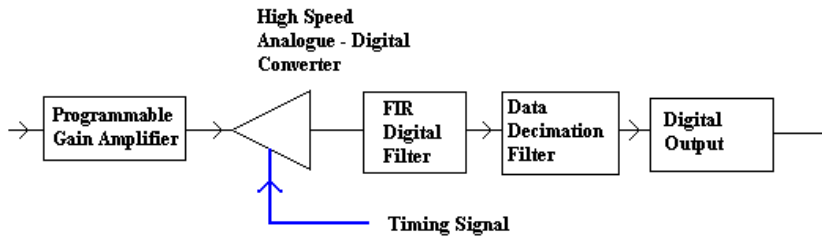


Figure 3 Sigma Delta Converter

The reason why over high sampling makes the Sigma Delta ADC ideal for analogue measurements is that for all practical purposes an external anti-alias filter are not required. Anti-alias filters when used in the context of data acquisition systems are used to prevent out of band signals from corrupting the measurements.

Figure 4 shows a typical frequency response for the pass band of the Sigma Delta ADC. The internal digital filters remove the dead band frequency components as would be detected by the high speed ADC. A simple passive R-C filter is used to remove any further noise which may be present. The R-C filter can be seen installed on the front end of the NetPod analogue input modules.

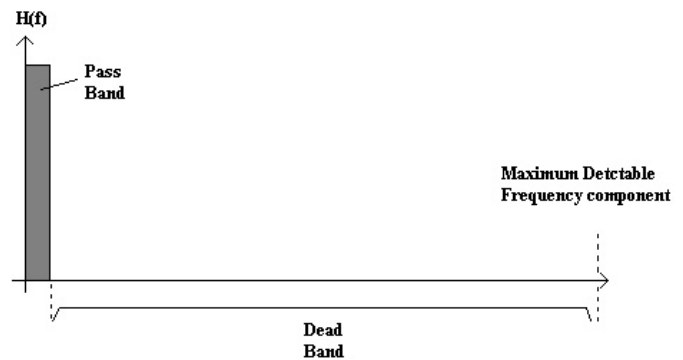


Figure 4 Typical Frequency Response Sigma Delta ADC

Data Acquisition Operations

The ADC acquires individual samples at a very fast rate compared to the input signal being investigated. The input samples are passed to a series of digital FIR filters that are combined to form a low pass anti-alias filter. When over sampling at the rate the Sigma Delta ADC undertakes it's operations, no input signal outside the bandwidth under investigation is deemed to exist and its effects on the Sigma Delta conversion is negligible even if present. Each filter removes unwanted out of bounds signals, and by combining multiple filters together high roll off rates can be achieved.

The digital FIR filters are used to remove the out of band frequencies and to undertake the data reduction using the correct mathematical procedures. It is not as simple as simply deleting data points when undertaking data reduction and care must be taken to undertake this task correctly in order to prevent alias effects from being artificially generated. All the digital filters are hard coded into the ADC by the manufacturer.

Even though the ADC may be operating very fast the actual output of samples is at the correct sample rate.

AD1210U Digital Filters

A number of different 24 Bit Sigma Delta ADC converters are used by the NetPod 4000 system but all operate in essentially the same way. This report is based upon the 24bit TI ADS1210U 24 bit device. This ADC utilises a series of averaging filters functions to form a low pass digital anti-alias filter. Effectively 3 x averaging function filters are used sequentially forming a Sinc³ filter frequency response. The Fourier Transform of the averaging filter is a Sinc function in the frequency domain. Mathematically speaking convolution of the input signal with the filter impulse response function undertakes the filtering action of the input signal and this is equivalent of multiplying the frequency response of the filter with the frequency response of the input signal.

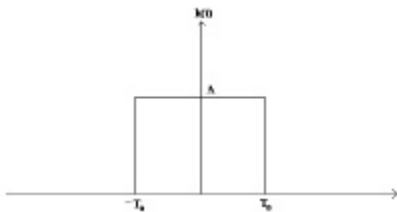


Figure 5 Averaging Function Digital filter

Frequency Domain

$$H(f) = 2 A T_0 \frac{\sin(2 \Pi f T_0)}{2 \Pi f T_0}$$

Time domain

$$h(t) = A \quad |t| < T_0$$

$$= A/2 \quad |t| = T_0$$

$$= 0 \quad |t| > T_0$$

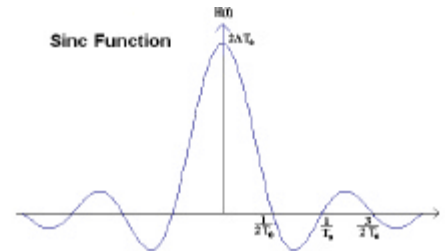


Figure 6 Frequency Response (Sinc Function)

An ideal digital filter will contain an infinite number of filter coefficients, however this in practice is not possible and so some degradation on the filtering action occurs. The effects of the constants in the above equations show how the amplitude of the frequency response can be used to include gain into the system. In practice the results provide a unity gain that is corrected within the calibration procedure.

Figures 5 and 6 shows the characteristics of the Sinc function digital filter. Figure 5 shows the shape of the filter as it appears as a series of coefficients in the time domain. Figure 6 shows the filter characteristics in the frequency domain. The low pass filter action occurs from DC ($2AT_0$ on the Y axis) to the first zero crossing point on the X-axis ($1/2T_0$). Careful selection of the 0 crossing point frequencies can be used to remove mains components on any input signals.

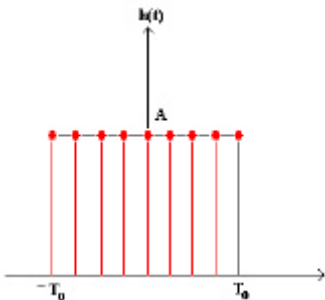


Figure 7 Filter Coefficients Averaging Filter

Figure 7 shows how the typical filter coefficients are obtained from the Averaging filter function. The closer the time interval between coefficients then the higher frequency the null crossing points appear in the filter frequency response.

The digital filter operations within the ADS1210U takes the average, of the average, of the average and presents this as the output value. Apart from being a very good low pass filter, the averaging process ensures a very good signal to noise ratio for signals within the pass band of the acquisition operations. The averaging process is used to reduce the overall sample rate to the desired rate.

Apart from undertaking the anti-alias operations within the digital filters the data rate is also decimated to the specified levels. The data decimation is also undertaken internally within the ADS1210 ADC. Due to the way the filters operate high dynamic ranges are often achieved with this type of ADC.

Step Response to Sinc³ Digital Filter

One of the important features of any digital filter system is the **Step Response**. This is the effect on a signal passing through the filter when a sudden change is applied to the input. This sudden change can be in the form of a signal going from 0V to full scale input or in fact any other sudden change in input level.

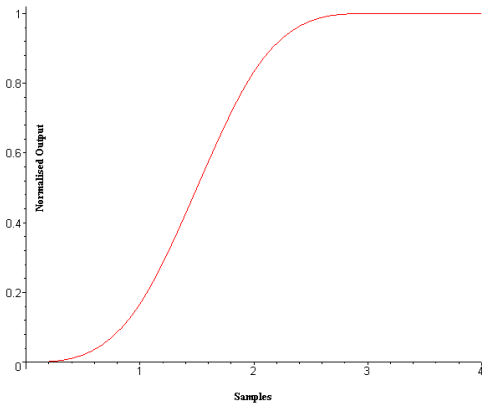


Figure 8 Sinc³ Step Response

Figure 8 shows the Step Response of the Sinc³ filter used with the NetPod 4000 analogue input modules. As can be observed it takes 3 samples, no matter the actual rate of acquisition for the filter to reach its steady state level.

At 1 KHz sample rate it will take approximately 3 ms for the instrument to go from 0 to Full scale (10V) for the high impedance card.

Any low pass anti-alias filter even those made from discrete components will have a very similar step response to that shown in Figure 7. The main advantage of using the digital anti-alias filter is that they will have identical properties for each input channel and will remain constant throughout the life of the instrument.

In practice the step response of the filter is hardly noticed in the characteristics of a signal measured by the Sigma Delta ADC. A straight forward sampling ADC can settle faster than a Sigma Delta ADC after the application of step input but may require external filtering to prevent out of band noise from corrupting results. On sampling ADC systems ringing can occur after the application of a step input for a short period until the ADC settles to the steady state.

The step response is a good measure of the overall effects of the digital filter system. The results of the step response are frequently shown as the number of samples required for the filter system to settle to the steady state level. Ideally the number of samples should be small. For the Sinc³ filter only 3 samples are required so this type of filter is very suitable for dynamic data acquisition systems applications.

Digital FIR Filters (Finite Impulse Response)

The digital filters within the ADS1210U use an FIR type filter. FIR stands for Finite Impulse Response and has the mathematical form:

$$y[n] = \sum_{k=0}^{M} b_k x[n-k]$$

For the FIR filter the output only depends past and present data values only making them ideally suited to be implemented in stand-alone devices such as ADC applications.

Advantages of FIR Filters

- 1) A FIR filter is inherently stable so there is no danger that inaccuracies in the filter coefficients may lead to instability.
- 2) FIR filters can be symmetrical in form (See Fig 6) and this produces an ideal linear-phase characteristic equivalent to a pure time delay of all frequency components passing through the filter. There is said to be no phase distortion of a signal when passing through and FIR.

Using multiple filters a high roll off rate from the pass band to the dead band can be achieved.